UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,199	03/16/2004	Ka Leung Ling	US00 0192 USA	3761

65913 7590 09/04/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
HASSAN, AURANGZEB	
ART UNIT	**PAPER NUMBER**
2182	

NOTIFICATION DATE	DELIVERY MODE
09/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/802,199
Filing Date: March 16, 2004
Appellant(s): LING ET AL.

Kenneth D. Springer Reg. No. 39,843
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/16/2008 appealing from the Office action mailed 1/15/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,513,374	Baji	4-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21- 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Baji (US Patent Number 5,513,374).

As per claims 21,41 and 42, Baji teaches a microcontroller, station and system that supports a plurality of message objects (instruction requests are the message objects), comprising: a processor core that runs applications (DSP core 3500, figure 1); a module that processes incoming messages (DMAC 3000 processes instructions over buses, figure 1); data memory (data memory is comprised of two segments: 1st - data 1900 and instruction 1400 memory, figure 1 and the 2nd – memory mapped registers internal to the DMAC, figure 4B) including a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects (1st segment is the plurality of buffers comprised in the data memory 1900 and the instruction memory 1400, figure 1), and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects (2nd segment is the plurality of memory-mapped registers seen in figure 4B), the memory-mapped

registers for each message object containing respective command/control fields for configuration and setup of that message object (memory mapped column 5, lines 54-64); and, a memory interface unit (the memory interface unit is the Parallel Arbiter 2100, figure 1 by which memory is interfaced through the unit comprising interface 2000 and interface 2400 and the DMAC, figure 1) that permits the processor core and the module to concurrently access a different respective one of the first and second memory segments (column 5, lines 7 -23), and that arbitrates access (column 5, lines 65 - 67 and column 6, lines 1 – 3) to the same one of the first and second memory segments when the processor core and the module request concurrent access to the same one of the first and second memory segments (concurrent access and conflicts thereof, column 6, lines 4 - 32, solution through arbitration rules, column 7, lines 1 -34).

The Examiner notes a message object according to the specification of the instant application can be considered to be a communication channel over which a complete message, or a succession of messages, can be transmitted (paragraph [0028]) and Baji teaches the channels for messages in figure 1 accordingly.

As per claims 28, 35, 37, 38 and 40, Baji teaches a microcontroller and method that supports a plurality of message objects (instruction requests are the message objects), comprising: a processor core that runs applications (DSP core 3500, figure 1); a module that processes incoming (DMAC 3000 processes instructions over buses, figure 1), wherein the processor core and the module are contained on a single

integrated circuit chip (figure 1); data memory including a first memory space (first data memory is comprised of two segments: 1st - data 1900 and instruction 1400 memory, figure 1 and the 2nd – memory mapped registers internal to the DMAC, figure 4B) that is located on the integrated circuit chip and a second memory space that is located off the integrated circuit chip (second data memory space is comprised of memory mapped registers in external memory 2500, figure 1), the first memory space including a first memory segment that provides at least a portion of a message buffer memory space that includes a plurality of message buffers associated with respective ones of the message objects (1st segment is the plurality of buffers comprised in the data memory 1900 and the instruction memory 1400, figure 1), and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects (2nd segment is the plurality of memory-mapped registers seen in figure 4B), the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object (memory mapped column 5, lines 54- 64); and, a memory interface unit (the memory interface unit is the Parallel Arbiter 2100, figure 1 by which memory is interfaced through the unit comprising interface 2000 and interface 2400 and the parallel I/O interface 4000, figure 1) that permits the processor core and the module to concurrently access a different respective one of the first and second memory spaces (concurrently access on and off-chip memory spaces, column 5, lines 7 -23), that permits the processor core and the module to concurrently access a different respective one of the first and second memory segments (the Parallel Arbiter 2100, figure 1 by which memory is interfaced through the

unit comprising interface 2000 and interface 2400 and the DMAC, figure 1), and that arbitrates access to the second memory space and that arbitrates access to the same one of the first and second memory segments when the processor core and the module request concurrent access to the second memory space or to the same one of the first and second memory segments (concurrent access and conflicts thereof, column 6, lines 4 - 32, solution through arbitration rules, column 7, lines 1 - 34).

As per claims 22 and 29, Baji teaches a microcontroller wherein the incoming messages include multi-frame, fragmented messages, and the module automatically assembles the multi-frame, fragmented messages (figures 3B and 3C show the multi-frame fragmented instruction requests handled).

As per claims 23 and 30, Baji teaches a microcontroller wherein the module includes the memory-mapped registers (figure 4B, column 15, lines 16- 19).

As per claims 24 and 31, Baji teaches a microcontroller wherein the processor core, the module, and the memory interface unit are contained on a single integrated circuit chip (figure 1).

As per claim 25, Baji teaches a microcontroller wherein the first and second memory segments are contained on the integrated circuit chip (figure 1).

As per claims 26 and 33, Baji teaches a microcontroller wherein the memory interface unit includes two independent arbiters (consists of more than two arbiters, figure 2).

As per claims 27, 34, 36 and 39 Baji teaches a microcontroller wherein the memory interface unit arbitrates access according to an alternate winner policy, wherein a previous loser is designated a current winner (initial access is granted based upon a priority scheme, and succeeding accesses are stalled and done in order of receipt, column 7, lines 1 - 34).

As per claim 32, Baji teaches a microcontroller wherein the second memory space provides at least a portion of the message buffer memory space (second memory is included in the overall memory space by the DSP, column 5, lines 54 - 65).

(10) Response to Argument

Appellant's arguments in the brief filed 6/16/2008 have been fully considered but they are not deemed to be persuasive.

The Appellant argues:

On page 9 of 26, lines 8 – 15 *"At the outset, in the Office Action of 15 January 2008, it appears that the Examiner cannot make up his mind as to what exactly he thinks in Baji corresponds to the recited objects.*

On paragraph 6, lines 2 – 3, he states that 'instruction requests are the message objects.' Then, on page 5, he states that: 'a message object according to the specification can be considered to be a communication channel over which a complete message, or a succession of messages, can be transmitted (paragraph [0028]) and Baji teaches the channels for messages in figure 1 accordingly.' "

Examiner's response:

The Examiner respectfully disagrees. The appellant's argument is direct to an Examiner's note cited to better elaborate the rejection of the independent claim 21 of the current application. The citation of paragraph 0028 **from the specification of the current application 10/802,199** was noted to the appellant for better understanding of what is necessitated by the claims. The citation was merely provided to assist in advancing prosecution and provide a **comparison** of the instant invention as set forth by the current application with respect to the prior art, **Baji**, under which the application was rejected. Paragraph 0028 of the Appellant's specification corresponds to page 5 lines 20 - 36 to page 7, line 29 as seen in the file wrapper. Although it is evident the Appellant has not thoroughly assessed the Examiner's note of what is necessitated by claims as deemed pertinent by the current application's specification, the claims will be addressed as best enabled by the specification.

The Appellant argues:

On page 10 of 26, lines 9 – 14 "*At the outset, Applicant notes that Baji teaches that the registers of FIG 4B – which the Examiner states supposedly correspond to the second memory segment – are internal registers to the DMA controller (DMAC) 3000 – which the Examiner states supposedly corresponds to the module of claim 1. The Examiner also states that DSP core 3500 supposedly corresponds to the recited processor core.*"

Examiner's response:

The Examiner respectfully disagrees. The Appellant's argument above is directed to the structural placement of the second memory and the Examiner interprets the Appellant's argument as a statement that the second memory segment cannot be internal to the DMA Controller because of access to the memory.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the first and second memory segments are "external" to both claimed processor core and module) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore the Examiner emphasizes the specification **of the current application** recites a processor core 22 which directly accesses a second memory segment 40 which is internal to the module 77 as seen in figure 3 and explicitly

described on page 21, lines 5 – 21 (also seen as paragraph 0116 of the printed publication of the current application). **The specification of the current application recites a structure of a second memory segment directly analogous to the reference Baji cited by the Examiner which the Appellant has dutifully repeated in the majority of the arguments presented as a drawback of Baji.**

The Examiner does not clearly understand the stance of the Appellant because on pages 10, 11 and 14 of the Appeal brief, the Appellant has provided resounding emphasis on the structural relationship of **Baji**'s second memory segments. It is best interpreted by the Examiner in light of the specification that the Appellant is in full agreement that the structure of **Baji** clearly anticipates the claims.

The Appellant argues:

On page 10 of 26, lines 21 – 30 "*…it is clear that the parallel arbiter 2100 of Baji absolutely does not permit DSP core 3500 and DMAC 3000 to concurrently access a different respective one of the first and second memory segments – where the second memory segments are the registers of FIG 4B (internal registers to DMAC 3000) as cited by the Examiner. It is also clear that parallel arbiter 2100 of Baji absolutely does not arbitrate access to the same one of the fist and second memory segments… when the DSP core 3500 and DMAC 3000 request concurrent access to the same one of the first and second memory segments.*"

Examiner's response:

The Examiner respectfully disagrees. In light of the previous response to argument regarding the emphasis of **Baji's** memory structure the Examiner notes that the concurrent access as set forth by the parallel arbiter is clearly defined in the rules established by **Baji** as seen in column 7. **Baji** teaches that all memory mapped locations can be independently accessed by both the DMAC 3000 and the DSP Core 3500, and parallel arbiter acts as an interface to handle the access and arbitrate in instances of concurrent access to the same memory segments as seen in column 5, lines 54 – 64. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Clearly one of ordinary skill in the art would recognize by **Baji's columns 5 - 7** citation of the parallel arbiter that the DSP Core and the DMAC have interfaced and arbitrated access to the first and second memory segments.

Furthermore assuming arguendo, all elements germane to the prior art are relevant including the additional memory segments recited by **Baji** which are also accessible by both 3000 and 3500 and interfaced via parallel arbiter 2100. Such memory segments include but are not exclusive to 2500, 1400, 2300 and 1900 of figure 1.

The Appellant argues:

On page 11 of 26, lines 1 – 4 *"Indeed, it does not appear that DSP core 3500 ever requests any access to the second memory segments … as alleged by the Examiner."*

Examiner's response:

The Examiner respectfully disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., processor core requests access to the second memory segment) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claims do not necessitate a positive recitation of a processor requesting a second memory segment. The Appellant argues lack of citation of elements which are not directly claimed. The claim limitations require an arbitration mechanism ***if and when*** a processor may request a second memory segment for which the Examiner has clearly cited the parallel arbiter 2100 with the accompanying rules seen in column 7. Clearly one of ordinary skill in the art would recognize that **Baji** teaches the ability to handle requests made by the processor to access first and second memory segment requests.

The Appellant argues:

On page 11 of 26, lines 18 – 22 *"The Examiner does not identify which of the many registers shown in FIG 4B of Baji supposedly contain respective command/control fields for configuration and setup of message objects (and again, as noted above, the Examiner does not clearly and consistently identify what are supposed to be the message objects in Baji in the first place)."*

Examiner's response:

The Examiner respectfully disagrees. The Examiner has explicitly cited in the rejection that the message objects are the instructions which are handled by the system. Furthermore figure 4B clearly shows the command/control fields for the instructions. The Appellant is directed to tables 1 and 2 seen in columns 10 - 12 of Baji to better understand the breakdown of an instruction which is handled by the plurality of registers seen in figure 4B. The claim limitations necessitate a plurality of memory mapped registers which is clearly reflected by the plurality of registers seen in the figure. The citation of column 5, lines 54 – 64 was included in the rejection to exemplify that the memory segments of Baji consist of memory mapped registers as necessitated by the claims. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Clearly one of ordinary skill in the art would be able to recognize that the command/control fields of the memory – mapped registers of **Baji's** as seen in figure 4B handle the setup of message objects - *instructions* as supported by the specification.

The Appellant argues:

On page 13 of 26, lines 3 – 6 *"The Examiner fails to explain how or why he believes that these timing operations illustrate that incoming messages include multi-frame, fragmented messages. More particularly, how can the timing diagrams of FIGs. 3B-C illustrate that the module automatically assembles the multi-frame, fragmented messages?"*

Examiner's response:

The Examiner respectfully disagrees. The Appellant's arguments are with respect to claim 22 which directly depends from claim 21. In the claim 21 the Examiner rejected the message objects in light of the instructions taught by Baji. Upon further examination of the instructions one of ordinary skill in the art would clearly recognize the that instructions are multi-frame, fragmented instructions as seen in tables 1 and 2 in columns 10 - 12. The timing diagrams were merely cited to show the functionality of automatic assembly in utilization of the instructions. The module DMAC 3000 as expressed in the above rejection and Examiner's responses handles the instructions, column 8, lines 9 – 22.

The Appellant argues:

On page 13 of 26, lines 14 – 26 *"Applicant respectfully submit that Baji does not disclose such a feature. The Examiner states that Baji does not disclose such a feature at col. 7, lines 1 – 34. Applicant's are confident that it will be apparent to the Board that:*

(1) the cited text teaches that arbitration for DSP Core 3500 and DMAC 3000 are ***independent*** *(not "alternating winner") and are based on a specific priority scheme spelled out on col. 7, lines 5 - 9; and (2) contrary to the Examiner's statement in the FINAL Office, the cited text does not disclose that only an* ***INITIAL ACCESS*** *is granted based on a priority scheme and succeeding accesses are done in order of receipt."*

Examiner's response:

The Examiner respectfully disagrees. In the first two statements of the Appellant's argument regarding statements of disclosure by the Appellant and Examiner render the statement confusing. The Examiner has not stated anywhere in the rejection of elements not disclosed by Baji any such statement would prove counterintuitive. The Appellant states that the arbitration done by **Baji** is **independent** and based on a specific priority scheme directly which ignores the claim limitations and the elements cited from **Baji**. The Appellant has only cited facts from rule 2 of **Baji** and has deliberately ignored **Rule 1** as seen in lines 1 - 4 of column 7. **Baji** states that when the two elements attempt concurrent access to the same memory segment and alternating policy is employed. The remaining citation from Rule 2 provided by the Appellant including the term **independent** is directed to memory accesses that are not concurrently requesting the same memory segment. The citation of **Baji** has been directly taken out of context through a piecemeal analysis of the reference **Baji** provided by the Appellant in support of arguments.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., arbitration is required in instances where the processor core and the module concurrently access a different respective one of the first and second memory segments) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is evident that the claim limitations necessitate a processor core and module that have **independent** arbitration schemes when vying for access to a different respective one of the first and second memory segments. Furthermore the arbitration scheme as described in claim 27 is **only limited to the arbitration for access to same one of the first and second memory segments.** Any arguments with respect to offshoot arbitration mechanisms are not necessitated by the claim limitations. Clearly one of ordinary skill in the art would recognize the **Baji** clearly anticipates an alternating winner policy when arbitrating access between a processor core and module vying for the same memory segment.

The Appellant argues:

On page 17 of 26, lines 16 – 22 *"The Office action merely states that 'broadening would dictate obviousness' and presents a table that identifies which claims of the*

present application the Examiner believes present a double-patenting situation with respect to which claims of the four cited patents. Applicants respectfully submit that this approach ignores the detailed analysis required under M.P.E.P. 804(II)(B)."

Examiner's response:

The Examiner respectfully disagrees. The double patenting rejection mapped out accordingly the claims from prior art that mapped directly to the instant application. In particular US Patent Number 6,732,255 recites all of the claim limitations verbatim with the exclusion of a single word CAN which in turn broadens the claimed environment and is deemed obvious. Furthermore the Examiner pointed out the claims were substantially the same as the US Patents 6715001, 6493287 and 6647440 with the exception that the instant application doesn't have the CAN microcontroller environment therefore broadening would dictate obviousness.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Aurangzeb Hassan
Patent Examiner
Art Unit 2182

Conferees:

/Tariq Hafiz/
TC2100 Supervisory Patent Examiner
Art Unit 2182

/Vincent F. Boccio/
Primary Examiner, Art Unit 2169
Appeal Practice Specialist TC2100